Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **A1**
2. **B1**
3. **NC**
4. **C1**
5. **D1**
6. **Y1**
7. **GND**
8. **Y2**
9. **A2**
10. **B2**
11. **NC**
12. **C2**
13. **D2**
14. **VCC**

**14**

**1**

**8**

**7**

**13 12 11 10 9**

**2 3 4 5 6**

**F20**

**A32S**

**MASK**

**REF**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential:**

**Mask Ref: A32S**

**APPROVED BY: DK DIE SIZE .036” X .040” DATE: 6/28/22**

**MFG: MOTOROLA THICKNESS .015” P/N: 54F20**

**DG 10.1.2**

#### Rev B, 7/19/02